Requirements, Constraints, and Engineering Standards

Team: sddec23-08

Problem Statement

Ideal:

- Iowa State University would have access to fabricated ReRAM chips for research purposes
- Iowa State University would have institutional knowledge of how the analog design flow works for the Skywater 130nm process

Reality:

- It is difficult to get any fabricated chip, especially one with ReRAM, because of how new of a technology it is.
- Iowa State University has never produced a fabricated analog chip on the Skywater 130nm processed

Consequences:

- It's difficult to do novel research that involves ReRAM because of the lack of fabricated chips.
- It's very difficult for students and faculty to create analog chips using the Skywater 130nm process because of the poor public documentation and the lack of internal documentation.

Proposal:

- Use eFabless's MPW shuttle program to submit a ReRAM chip proposal.
    - If it gets approved, it would give us access to fabricated ReRAM chips
    - Along the way, we would document our workflow, contributing the ISU's internal knowledge of analog fabrication in the Skywater 130nm process.

Requirements & Constraints

- **Functional**
  - Create an eFabless submission
  - Create a ReRAM crossbar
  - Create the infrastructure necessary to communicate with the crossbar through memory mapped registers
  - Allow the crossbar's inputs and weights to be modified.
- **Qualitative**
  - Is able to quickly compute multiply and accumulate operations
  - Create documentation for the tool flow required to create the submission
- **UI Requirements**
  - Write drivers so it's easier for programmers to interact with the crossbar

Engineering Standards

- **IEEE 1481-2019 - IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)**
  - Standard created for setting expectations for timing and power simulations for integrated circuits using design automation (EDA) tools

- **IEEE 1076.4-2000 - IEEE Standard VITAL ASIC Modeling Specification**
  - Standard created for testing and simulating ASIC chips

- **IEEE 1149.4-2010 - IEEE Standard for a Mixed-Signal Test Bus**
  - Standard created for simulating digital and analog devices both independently and together

Intended Users and Uses

- Professor Wang will find this project beneficial for research involving ReRAM.
- Efabless will find this project useful if it gets selected as an MPW submission since it will allow them to refine their fabrication processes.
- Professor Duwe and future CprE 491/492 students will find this project useful since it will provide additional documentation for open source tooling for analog open source design and fabrication tools.